REMARKS

Claims 1 - 6, 8, and 10 - 13 remain pending in the present application, of which claims 1, 6 and 8 have been amended. Applicant respectfully submits that no new matter has been added. It is therefore believed that this Amendment is fully responsive to the Office Action dated **January 28, 2003**.

ALLOWABLE SUBJECT MATTER:

Applicants gratefully acknowledge the indication in item 13 of the Office Action that claims 4, 5 and 10 - 13 are allowed.

AS TO THE MERITS:

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1 - 3 and 8 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ushiku, et al. (U.S. Patent No. 5,032,890).

2) claims 1 and 6 stand rejected under 35 U.S.C. §102(b) as being anticipated by Bothra, et al. (U.S. Patent No. 6,020,616); and

3) claim 8 stands rejected under 35 U.S.C. §103(e) as being anticipated by Shin (U.S. Patent No. 6,384,464).

Each of these rejections is respectfully traversed.

Independent Claim 1:

Ushiku is directed to addressing difficulties in forming a pattern on the insulating film 60 that is not flat at positions where no interconnection layer pattern is provided (Fig. 4B). In Fig. 7, dummy patterns 20, 30a - 30c, and 40 are provided where patterns 22, 32, and 42 are not located, thereby making it possible to form a flat insulating film on top of these patterns. On this insulating film, patters 201 and 205 are provided as upper-layer patterns.

In Ushiku as described above, the dummy patterns and the patterns 22, 32, and 42 are provided in the same layer, with the upper-layer patterns 202 and 204 being formed on the dummy patterns.

Accordingly, Ushiku does not teach providing wire dummies in a second layer different from a first layer by avoiding areas that are directly above or below positions of wires provided in the first layer.

Bothra shows, in Fig. 3L, active regions (transistors) 204, dummy active regions 214, polysilicon gates 216, and dummy polysilicon lines 226. The examiner asserts that the dummy polysilicon lines 226 are formed in non-overlapping relationship to active regions 204 of the substrate and in non-overlapping relationship to the active wiring network (polysilicon gates 216).

As shown in Fig. 2B, the dummy polysilicon lines 226 and the polysilicon gates 216 are formed in the same layer.

Accordingly, Bothra does not teach providing wire dummies in a second layer different from a first layer by avoiding areas that are directly above or below positions of wires provided in the first layer.

Independent Claim 8:

Neither, Ushiku nor Shin teaches square dummy patterns having different sizes and arranged at respective different pattern intervals.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/994,753

IN THE CLAIMS:

Claims 1, 6 and 8 have been amended to read as follows:

1. (AMENDED) A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer by avoiding areas that are directly above or below positions of said wires provided in said first layer [and having an arrangement that avoids areas overlapping positions of said wires].

6. (AMENDED) The semiconductor integrated circuit as claimed in claim 1, wherein said wire dummies [have the arrangement that further avoids areas overlapping] further avoid areas that are directly above positions of polysilicon or diffusion layers.

8. (TWICE AMENDED) A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

square dummy patterns provided in said wire layer and having different sizes,

wherein said square dummy patterns having different sizes are arranged at respective different pattern intervals.